APPENDIX

CLAIMS 2, 3, 5 - 8, 21, 22, AND 26 - 30, WITH ANNOTATIONS TO INDICATE REVISIONS, OF U.S. PATENT APPLICATION 10/045,137, ATTY DOCKET NO. NS-3868-2C US

2. (Twice amended) The ESD protection structure of Claim 8, wherein said first conductivity type is [an] n-type [semiconductor], and said second conductivity type is [a] p-type [semiconductor].

3. (Twice amended) The ESD protection structure of Claim 8, wherein said first conductivity type is [a] p-type [semiconductor], and said second conductivity type is [an] n-type [semiconductor].

5. (Three times amended) The ESD protection structure of Claim 8, wherein said third semiconductor region includes a well [an n-well] region of said first conductivity type formed in a [p-type] semiconductor substrate of said second conductivity type.

6. (Twice amended) The ESD protection structure of Claim 5, wherein each of said second and [said] fourth semiconductor regions includes [each include] a base [p-base] region of said second conductivity type formed in said well [n-well] region.

7. (Twice amended) The ESD protection structure of Claim 6, further including a pair of heavily doped semiconductor regions of said second conductivity type, each [wherein said first and said fifth semiconductor regions each include an n+ region] formed in a different one of said base [p-base] regions.

8. (Twice amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous [in contact] with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

an electrically floating third semiconductor region of said first conductivity type continuous [in contact] with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type continuous [in contact] with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type continuous [in contact] with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

[wherein] a first terminal[, A, of said ESD structure is] connected to said first [semiconductor region] and [said] second semiconductor regions [region];

[and] a second terminal[, K, of said ESD structure is] connected to said fourth [semiconductor region] and [said] fifth semiconductor regions [region];

a first resistor coupled between said first terminal and said second semiconductor region;

a first current source coupled between said terminals so as to be in series with said [connected to terminal A and a first end of a] first resistor [whose second end is connected to terminal K]; [and]

a second resistor coupled between said second terminal and said fourth semiconductor region; and

a second current source coupled between said terminals so as to be in series with said [connected to terminal K and a first end of a] second resistor [whose second end is connected to terminal A].

21. (Amended) An electrostatic discharge (ESD) protection structure for protecting an integrated circuit, said ESD protection structure, comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type continuous [in contact] with said first semiconductor region, said second conductivity type being opposite to said first conductivity type;

an electrically floating third semiconductor region of said first conductivity type continuous [in contact] with said second semiconductor region and separated from said first semiconductor region by said second semiconductor region;

a fourth semiconductor region of said second conductivity type continuous [in contact] with said third semiconductor region and separated from said second semiconductor region by said third semiconductor region;

a fifth semiconductor region of said first conductivity type continuous [in contact] with said fourth semiconductor region and separated from said third semiconductor region by said fourth semiconductor region;

[wherein] a first terminal[, A, of said ESD structure is] connected to said first [semiconductor region] and [said] second semiconductor regions [region];

[and] a second terminal[, K, of said ESD structure is] connected to said fourth [semiconductor region] and [said] fifth semiconductor regions [region];

[a first pair of back-to-back diodes one of which is connected to terminal A;]

a first resistor coupled between said first terminal and said second semiconductor region [connected to the other of the second pair of back to back diodes and to terminal K];

a first pair of back-to-back diodes coupled between said terminals so as to be in series with said first resistor;

[a second pair of back-to-back diodes one of which is connected to terminal K; and]

a second resistor coupled between said second terminal and said fourth semiconductor region [connected to the other of the second pair of back to back diodes and to terminal K]; and

a second pair of back-to-back diodes coupled between said terminals so as to be in series with said second resistor.

22. (Amended) The ESD protection structure of Claim 21, wherein said [first and second pair of back-to-back] diodes are [back-to-back] Zener diodes.

26. (Amended) The ESD protection structure of Claim 21 [25], wherein said first conductivity type is [an] n-type [semiconductor], and said second conductivity type is [a] p-type [semiconductor].

27. (Amended) The ESD protection structure of Claim 21 [25], wherein said first conductivity type is [a] p-type [semiconductor], and said second conductivity type is [an] n-type [semiconductor].

28. (Amended) The ESD protection structure of Claim 21 [27], wherein said third semiconductor region includes a well [an n-well] region of said first conductivity type formed in a [p-type] semiconductor substrate of said second conductivity type.

29. (Amended) The ESD protection structure of Claim 28, wherein each of said second and [said] fourth semiconductor regions includes [each include] a base [p-base] region of said second conductivity type formed in said well [n-well] region.

30. (Amended) The ESD protection structure of Claim 29, further including a pair of heavily doped semiconductor regions of said second conductivity type, each [wherein said first and said fifth semiconductor regions each include an n+ region] formed in a different one of said base [p-base] regions.